What Is Claimed Is:

1. An electronic circuit unit comprising:

an alumina substrate;

a thin film conducting pattern formed on the alumina substrate;

thin film circuit elements including capacitors, resistors, and inductance elements formed on the alumina substrate and connected to the conducting pattern; and

a semiconductor bare chip wire bonded to the conducting pattern,

wherein an area of a connection land on which the semiconductor bare chip is mounted is smaller than a bottom surface area of the semiconductor bare chip.

2. The electronic circuit unit according to claim 1, wherein at least two sides of the semiconductor bare chip are located apart from a contour of the connection land.

3. The electronic circuit unit according to claim 1, wherein an opening is formed in the connection land.

4. The electronic circuit unit according to claim

2, wherein an opening is formed in the connection land.

5. An electronic circuit unit comprising:

a first capacitor formed by laminating a first bottom electrode and a first top electrode with interposition of a first dielectric material on a substrate, and

a semiconductor bare chip mounted on the first capacitor,

wherein the first top electrode serves as a part of a connection land connected to a bottom side electrode of the semiconductor bare chip.

6. An electronic circuit unit comprising:

a capacitor formed by laminating a bottom electrode and a top electrode with interposition of a dielectric material on a substrate, and

a semiconductor bare chip mounted on the substrate,

wherein the top electrode of the capacitor is wire bonded to a top side electrode of the semiconductor bare chip.

7. The electronic circuit unit according to claim 5, wherein a second capacitor is formed by laminating a second bottom electrode and a second top electrode with interposition of second dielectric material on the substrate, wherein the second top electrode of the second capacitor is wire bonded to a top side electrode of the semiconductor bare chip.